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HW #3

2^N = Bytes of $ blk -> offset = N

2^M = total $ size /(# ways \* & blk size) -> index = M

Tag = 32 - N - M

A)

|  |  |
| --- | --- |
| Field | Size (bits) |
| Offset | 6 bits |
| Index | 12 bits |
| Tag | 14 bits |

B)

|  |  |
| --- | --- |
| Field | Size (bits) |
| Offset | 6 bits |
| Index | 0 bits |
| Tag | 26 bits |

C)

|  |  |
| --- | --- |
| Field | Size (bits) |
| Offset | 6 bits |
| Index | 10 bits |
| Tag | 16 bits |

2)

1. Calculate M & N based on cache architecture
2. Convert address to binary numbers (hex -> binary)
3. map/locate data based on architecture

A)

Direct Mapped

8 Sets

$ blk size 16 B

N = 4

M = 3

offset is right most 4 bits

index is 3 bits to the left of offset

tag is left most 5 bits

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Instruction | Iteration 1 | Iteration 2 |
|  | loop: |  |  |
| 0x108->  0001 0000 1000 | addiu r1, r1, -1 | Compulsory |  |
| 0x11c->  0001 0001 1100 | addiu r2, r2, 1 | Compulsory | conflict |
| 0x110->  0001 0001 0000 | j foo |  |  |
|  | ... |  |  |
|  | foo: |  |  |
| 0x218->  0010 0001 1000 | addiu r6, r6, 1 | Conflict | Conflict |
| 0x21c->  0010 0001 1100 | bne r1, r0, loop |  |  |

1. Conflict
2. Compulsory
3. Capacity

B)

Miss Rate = (3 + 31\*2) / (32\*5) = 65/160 = .40625

Time = IC\*CPI\*CycleTime

=(32\*5) \* (.40625\*6) \* 1/3

= 130

3) A)

Computer A: Time = IC\*CPI\*CycleTime

= 1.5 \* 1 \* ⅓

= .5

Computer B: Time = IC\*CPI\*CycleTime

= 1 \* 2 \* ¼

= .5

Speedup:

.5/.5 = 1

(1 - 1) \* 100 = 0%

Both computer A and B are equivalent therefore the speedup is 1 or 0%.

B)

Computer A: CPI = 1 + .03(15+.03(250)) + .3(.09)(15+.03(250))

= 1 + .675 + .6075

= 2.2825

Time = 2.2825 \* 1.5 \* ⅓

= 1.141

Computer B: CPI = 2 + .02(12+.04(300)) + .3(.05)(12+.04(300))

= 2 + .48 + .36

= 2.84

Time = 2.84 \* 1 \* ¼

= .71

Speedup:

1.141/.71 = 1.607

(1.607 - 1) \* 100 = 60.7%

Computer B is faster by 60.7%